

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Chen et al.

Title: Read and Erase Verify Methods and Circuits Suitable for Low Voltage Non-Volatile Memories

Application No.: 10/552,948 Filing Date: September 11, 2006

Examiner: Yoha, Connie C. Group Art Unit: 2827

Docket No.: SNDK.284US1 Conf. No.: 6573

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INTERVIEW SUMMARY**

Dear Sir:

A telephonic interview was held between the examiner, Connie C. Yoha, and the undersigned on May 19, 2008 with respect to the above captioned patent application. The interview was at the instigation of the examiner and consisted of a pair of telephone calls.

The examiner indicated the application, previously allowed, had been reviewed and that there were three issues raised.

A first issue discussed was the dependence of claims 36 and 37, which depended on a canceled claim. It was agreed that these claims could have their dependence changed, by examiner's amendment, to claim 30.

The second issue was that the examiner believed that there was a basis for an obviousness-type double patenting rejection with respect to US patent number 6,839,281. Although the validity of this rejection has not been considered in any detail, a corresponding terminal disclaimer is attached in order to facilitate the application process.

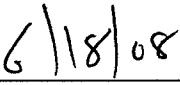
The third issue related to whether the independent claims, 20 and 30, were anticipated by US patent number 6,292,423. Although there was, at a general level, some agreement that what was being done in the present application differed from what is found in the reference, agreement was not reached as to whether such distinctions were found in the pending versions of the independent claims. The undersigned submitted that these claims, as pending, were not

anticipated, while the examiner thought they likely were, although she would consider them further in light of the discussion.

Respectfully submitted,

  
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Michael G. Cleveland

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Date

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